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DESIGN AND CONTROL OF MMC BASED HVDC GRID UNDER UNBALANCED VOLTAGE CONDITIONS

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Abstract- **Power electronics based solutions such as the Static Synchronous Compensator are increasingly deployed to mitigate power quality issues while High Voltage DC Transmission converters are currently installed to support the existing grid transmission capacity. Both applications require high power and high voltage power converters using switching devices with limited voltage ratings. The advent of Modular Multilevel Converters (MMC) is one of the recent responses to this need. These use half or full H-bridge circuits stacked up to form a chain, and hence can withstand high voltages using lower-rated switching devices. For high-voltage direct-current (HVDC) transmission, the strength of the ac system is important for normal operation. An ac system can be considered as weak either because its impedance is high or its inertia is low.**

A typical high-impedance system is when an HVDC link is terminated at a weak point of a large ac system where the short-circuit capacity of the ac system is low. This paper focuses on the control of Modular Multilevel Converters (MMC) for High Voltage DC (HVDC) applications during unbalanced AC grid voltage sags where positive and negative sequence voltages are equal. The control scheme is based on six arm energy regulators, six independent current controllers, and two reference calculation stages that convert the power references into grid and inner current references. Conventional inner AC currents reference calculation fails if the amplitude of the positive and the negative sequence AC grid voltages are equal, a state which is referred to in this paper as singular voltage condition. This paper discusses the types of network faults that cause this condition and proposes three different solutions to operate the converter in such scenarios. The adequacy of the proposed solutions is validated through matlab/simulink simulations considering each of the problematic fault scenarios.

***Index Terms*— HVDC transmission, modular multilevel converters, unbalanced operation, voltage-source converter.**

I. INTRODUCTION

Recent development has led to the implementation of modular multilevel cascaded converters (MMCCs), a new breed of power electronic converter. In a MMCC topology, a power module is used as a basic building block and multiple modules are stacked to meet an application's power level requirements. In this context, "power module" refers to a basic circuit configuration comprising semiconductor switches which are switched in or out of circuit to provide access to an energy storage device. The topology has no known extension limitations and commercial systems exist with such configurations, however the control of this topology introduces several challenges. By nature, the topology presents several current paths, thus during operation, phenomena termed "circulating currents" may occur.

The mitigation of this phenomenon is an active area of research in several institutes. Another key challenge involves maintaining balance in the energy storage element in each module as this is difficult in practice and requires sophisticated modulation algorithms, thus is also a subject of active research. Hitherto the basic building blocks in an MMCC as well as emerging parallel and series variants, for example, the Alternate Arm Converter (AAC), employed either half or full-bridge circuits with a capacitor. The review of the features of conventional multilevel converters, such as the diode clamped or flying capacitor types, suggests that it is possible to use any one or both of

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them as the building blocks for an MMCC, hence exploiting their advantages and increasing their range of applications to include higher power.

Several investigations have produced significant publications, and industrial applications are in existences which confirm the versatility of the MMC for medium to ultra-high power applications, making the MMC circuit architecture of primary interest in this research work. The operation of the MMC during unbalanced AC and DC grid conditions has also been studied. The specific case of the singular voltage condition, where positive and negative sequence of the AC grid voltages are equal, is highly problematic as it may result in singularities in the calculation of current references.

This situation has been studied in the past for two-level VSCs where the resulting low-frequency power ripple going into the DC bus was a concern. A similar problem arises in the MMC for both the AC grid and inner current reference calculation stages. The discussion introduced for AC grid currents reference calculation is also valid for MMCs. Regarding the inner current references, a solution based on applying offset voltage was presented for double line faults. In the present project, three alternative methodologies that enable the operation of the converter under all possible faults that cause the singular voltage condition are proposed.

The first methodology is based on disabling the problematic elements of the arm energy balancing controllers upon detection of the singular voltage condition. The two other methods are based on solving the current reference calculation problem using linear algebra tools for incompatible systems. In order to validate these methods, a detailed analysis of the different types of voltage sags that result in singular voltage conditions is developed. Simulations are carried out to demonstrate the performance achieved using the different methods.

II. MODULAR MULTILEVEL CONVERTERS

In an MMC topology, each converter phase comprises at least an "arm" built up from a stack of sub-modules. An inductor is normally inserted either at the top or bottom of the stack and this depends on physical installation limits such as the footprint available on site. This "buffer" inductor serves the purpose of limiting the in-rush current to the converter arm as well as limiting di/dt in the converter's current waveforms during the different switching actions.

A half-bridge cell comprises two switching devices, two diodes and a DC energy storage element (i.e. capacitor, super-capacitor or battery) as illustrated in Figure 1(a). Each cell is capable of producing a two state output voltage: 0 or $+VC$, where VC is the voltage of the associated DC source. Thus each cell acts as a controllable unipolar voltage source. The current flow through each cell can be bidirectional, hence it gives two quadrant operation. For high voltage applications, multiples of such cells are used as sub-modules and the terminals of these are cascaded to form one phase arm with the inductor mentioned above connected at one end as shown in Figure. 1(b).

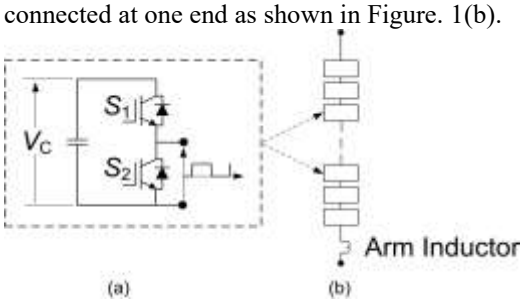

Fig:1. (a) Half-Bridge Cells and (b) one converter phase arm.

Since its inception, various names have been given to the modular multilevel topology, such as cascade multilevel converter, modular multilevel converter, M2LC, M2C and chain-link converter. To establish consistency, both in naming and understanding, a review and classification of this family of converters was conducted in 2010. In this review, the name "Modular Multilevel Cascaded Converters" (MMCC) was adopted for this family of converters. The following categories are specified within:

- Single Star Bridge Cells (MMCC-SSBC)
- Single Delta Bridge Cells (MMCC-SDBC)
- Double Star Chopper Cells (MMCC-DSCC)
- Double Star Bridge Cells (MMCC-DSBC)

Note that each of the converters in this category presents certain characteristics that either

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increase or reduce suitability when applied in one application or the other. To ensure consistency with existing literature, the term "arm" is used to refer to a cascade of modules that act together to synthesize the same portion of an output (AC or DC) in an MMC. The author is aware the other nomenclature such as converter "limb" or "phase limb" may be used in other literature. In the topologies described it is also assumed that the storage element used is a capacitor. In this thesis, the format adopted for discussing the MMCC family involves a further categorization into the following:

- No DC link (Single- Bridge Cells: SSBC, SDBC)
- Common DC link (Double Star- Cells: DSCC, DSBC)

The "No DC link" category includes the MMCC-SSBC and MMCC-SDBC circuits, while the Common DC link category includes the MMCC-DSCC and MMCC-DSBC circuits. Although the MMCC-SSBC and MMCC-DSBC are more popular circuits, especially for industrial implementation, all the categories are discussed in this section including the double delta circuit which was not reviewed.

III. SYSTEM MODELING

Fig. 2 shows the simplified diagram of a three-phase MMC. The converter has three phase units (known as legs) with two stacks of sub-modules (SM) in each, known as upper and lower arms. Each arm has *N*arm SMs, which in the basic MMC present a half-bridge topology. Each SM can be either inserted or by-passed, allowing the arm to behave as a positive controllable voltage source. The voltage applied by the arms is used to control their current, which in turn is used to transfer power and achieve internal energy balance in the converter.

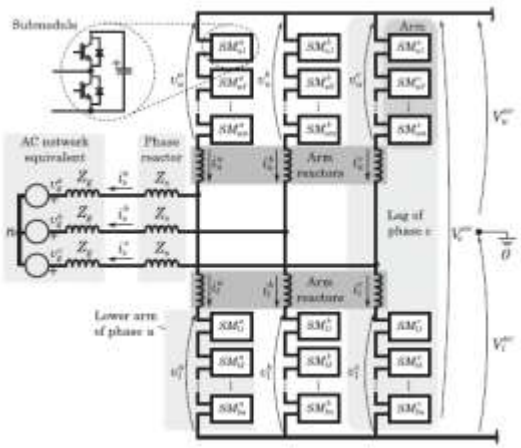

Fig:2. Complete scheme of an MMC converter.

The basic relevant variables of the converter are shown in Fig. 2: v^j_g is the grid voltage, v^j_u and v^j_l are the upper and lower arm voltages respectively and $V^{DC}{}_u$ and $V^{DC}{}_l$ are the voltages of the upper and the lower poles of the HVDC link. Also, another two variables that do not appear in Fig. 4.1, but play an important role in the energy balancing of the converter are the sums of the SM capacitor voltages of the upper and the lower arms v^j_{u-s} and v^j_{l-s}, respectively. The relevant currents are the grid current i^j_s and the upper i^j_u and lower i^j_l converter arm currents. Regarding the converter circuit impedances, *Ra* and *La* are the equivalent arm resistance and the inductance of the arm reactors respectively, *Rs* and *Ls* are the resistance and inductance of the phase inductors2 and *Rg* and *Lg* correspond to the equivalent impedances of the AC grid.

The control scheme employed (see Fig. 3) follows the design procedure introduced. *P*g* and *Q*g* are the AC grid active and reactive power references. The corresponding AC output current reference $i\alpha\beta0^*s$ is obtained through a reference calculation structure which takes into account unbalanced voltage situations while its DC component $i\alpha\beta0DC^*s$ is set to zero to prevent DC current flowing through the AC grid, for instance to avoid transformer saturation. In order to balance the internal energy of the converter, six separated energy control loops are required. Specifically, the controlled energy variables are the total energy of the converter *Et* the energy differences between the converter legs $E_{a\to b}$ and $E_{a\to c}$, and the energy difference between the upper and lower arms of the

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MMC $E^{j}_{l\rightarrow u}$. The output of the energy regulators are the power references $P^{*}t$, $P^{*}a\rightarrow b$, $P^{*}a\rightarrow c$ and $Pj^{*}l\rightarrow u$. These are fed to a reference calculation stage in order to obtain the additive AC $i\alpha\beta 0^{*}$ *sum* and DC current references $i\alpha\beta 0DC^{*}sum$, which are tracked using the current controllers. All current controllers are designed to track current references in the stationary frame containing AC and DC components.

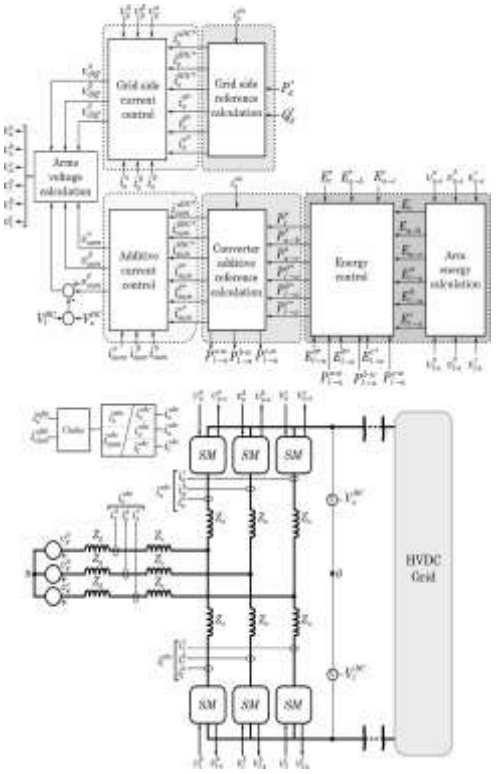

Fig. 3. Control structure of the MMC converter.

As mentioned in the previous section, three different regulators are in charge of balancing the energy difference between the upper and the lower arms within a phase unit$Ej\ l\rightarrow u$.

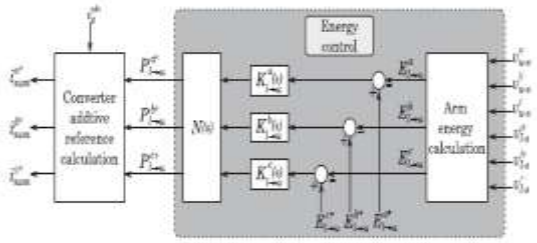

Fig. 4. Upper-lower arms energy balancing control structure.

Fig. 4 shows a possible implementation of these controllers which consists of three different PI compensators that can be designed to reject disturbances that may appear during the converter operation. Apart from the PI controllers, the scheme also includes a notch filter $N(s)$ to block sending line and double-line frequency magnitudes to the reference calculation stage, as the additive current references are obtained using only the average power values. Note that, the additive reference calculation stage could be combined with other energy regulator structures. For certain voltage conditions, the AC additive current reference calculation is not able to extract valid current references, affecting the energy balancing between the upper and lower arms.

The reference values of all components of the current are calculated from the power references given the instantaneous measured AC and DC grid voltages. A variation of the AC grid voltage causes the AC components to change, whereas a variation of the DC grid voltage causes the DC components to change. The choice of the AC grid current reference during an unbalanced voltage sag has been discussed in the past and the most common approach to date is to set its negative sequence to zero and to export active and reactive power using positive sequence current only. In such a scenario, the active power exchanged between each leg of the converter and the AC grid is different, resulting in a sustained drift of their energy that must be compensated using additive DC current. On the other hand, the additive AC current is normally used to control the differences between the energy of the upper arms and the energy of the lower arms, which may suffer from deviations during transients. This singularity causes the additive current references to saturate, which compromises the performance of the energy

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balancing controllers. This reference calculation problem could also appear for other control strategies different than the control scheme shown in Figure, provided that the control method uses AC additive currents to balance the energy stored in the upper and lower arms.

IV. SIMULATION RESULTS

CASE-A: Method 0 - Conventional control.

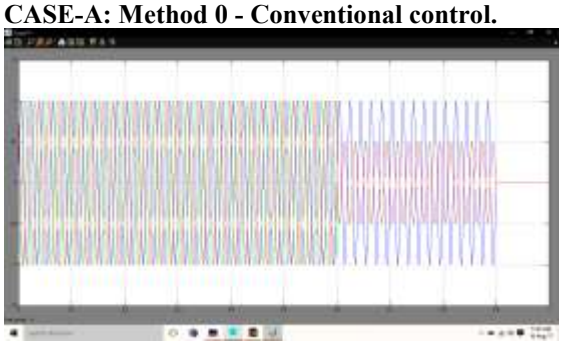

Fig:5(a) grid voltage

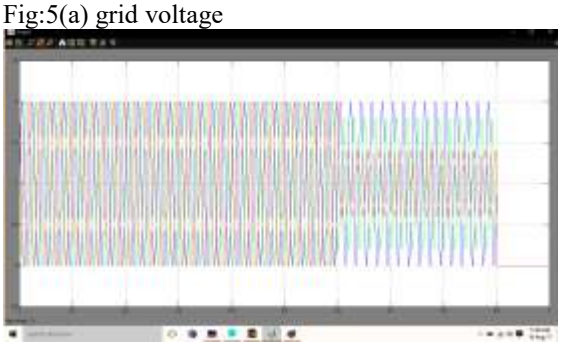

Fig:5(b) MMC upper arm voltage

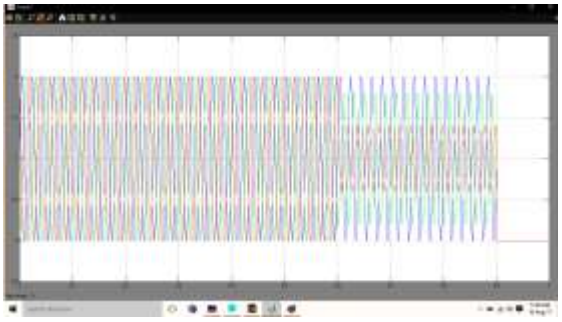

Fig:5(c) MMC lower arm voltage

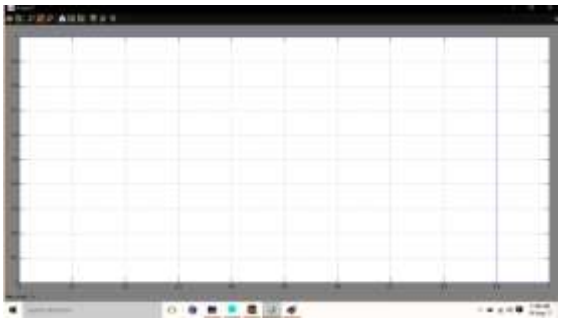

Fig:5(d) HVDC voltage

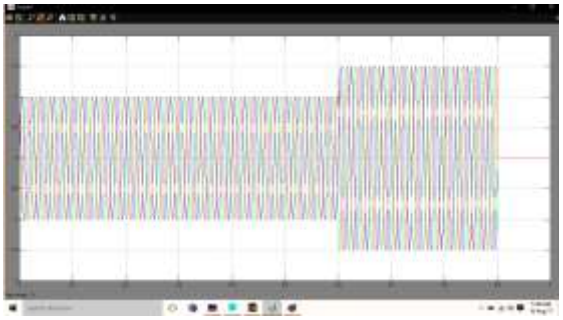

Fig:5(e) grid current

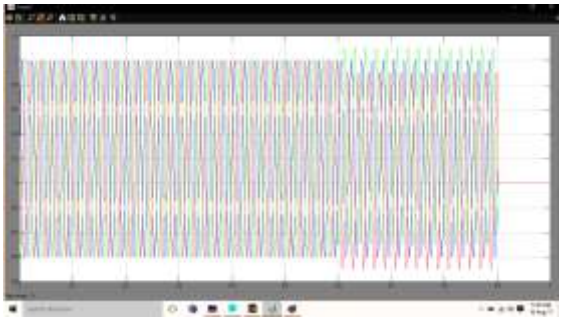

Fig:5(f) MMC upper arm current

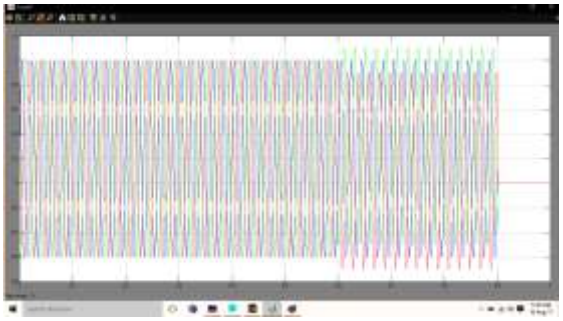

Fig:5(g) MMC lower arm current

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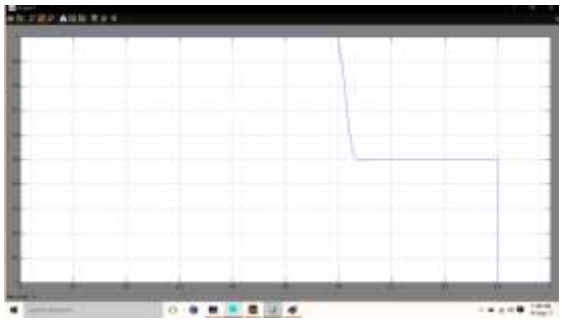

Fig:5(h) HVDC current

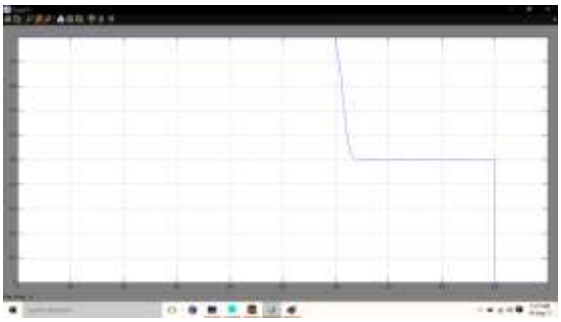

Fig:5(l) HVDC power

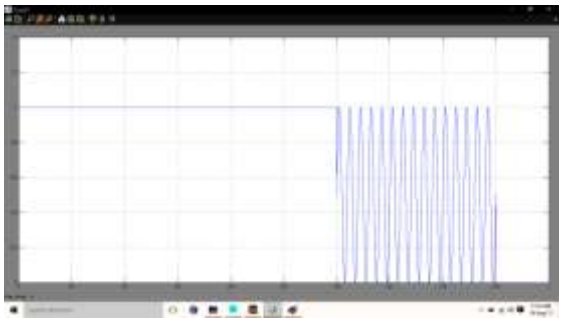

Fig:5(i) grid power

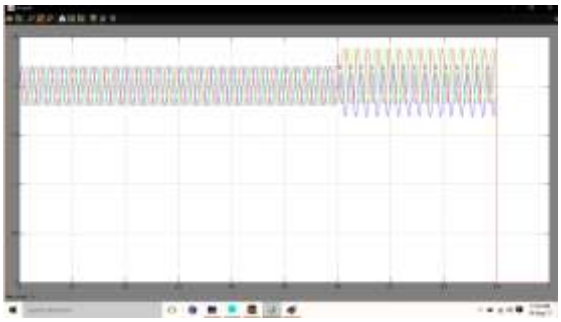

Fig:5(m) capacitor MMC upper arm

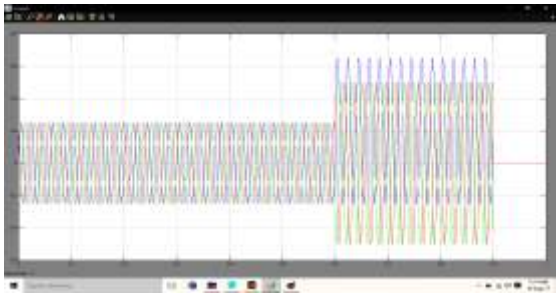

Fig:5(j) MMC upper arm power

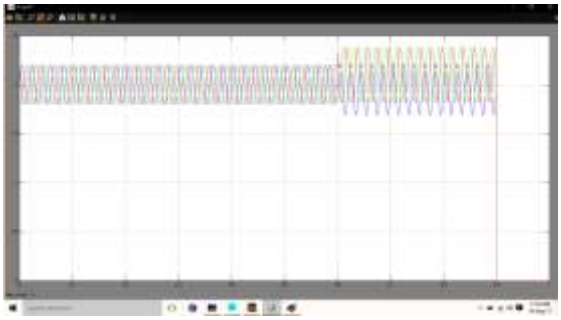

Fig:5(n) capacitor MMC lower arm

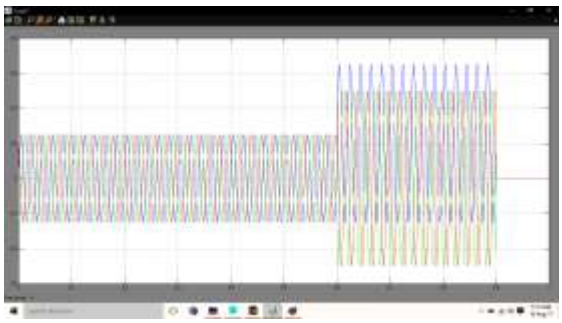

Fig:5(k) MMC lower arm power

Fig. 5. Simulation results of the MMC operation. Voltage sag type C. Method 0 – Conventional control.

CASE-B: Method 1 - Energy balancing disconnection

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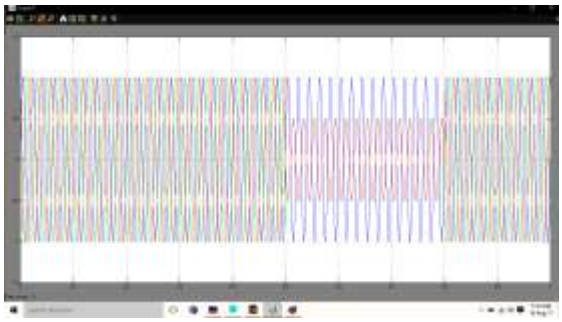

Fig:6(a) grid voltage

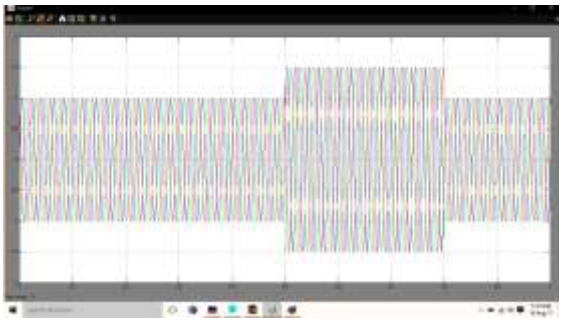

Fig:6(e) grid current

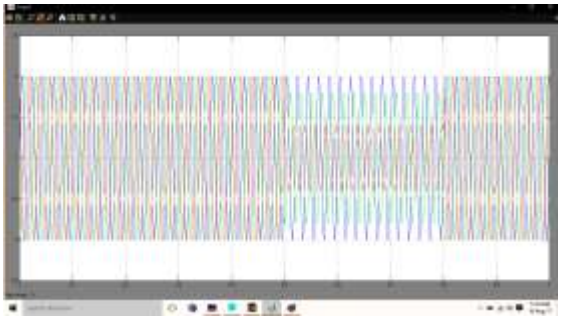

Fig:6(b) MMC upper arm voltage

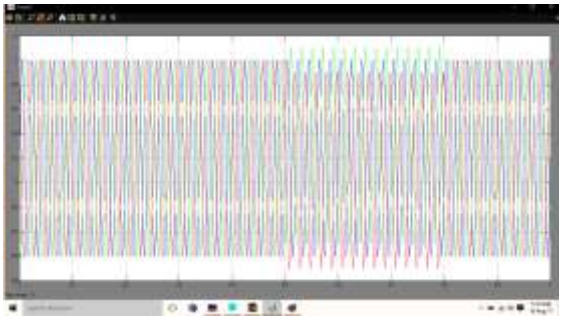

Fig:6(f) MMC upper arm current

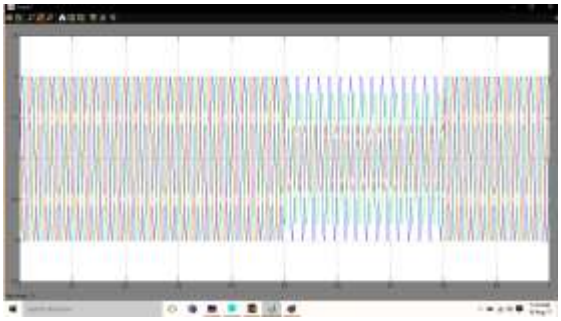

Fig:6(c) MMC lower arm voltage

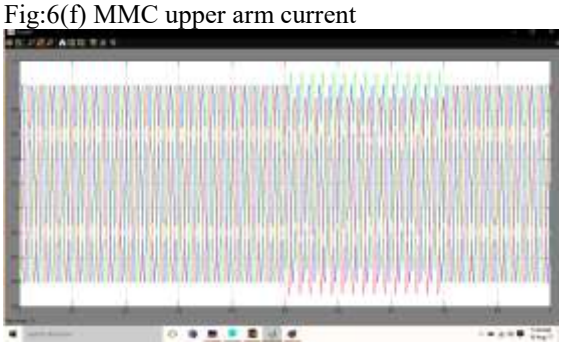

Fig:6(g) MMC lower arm current

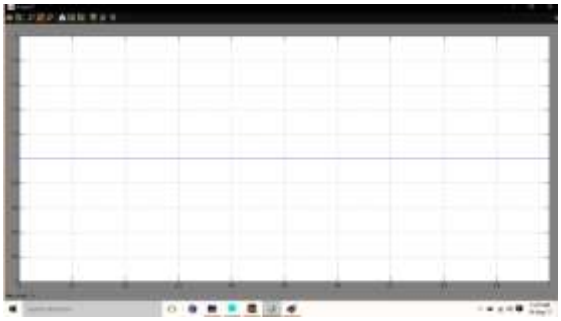

Fig:6(d) HVDC voltage

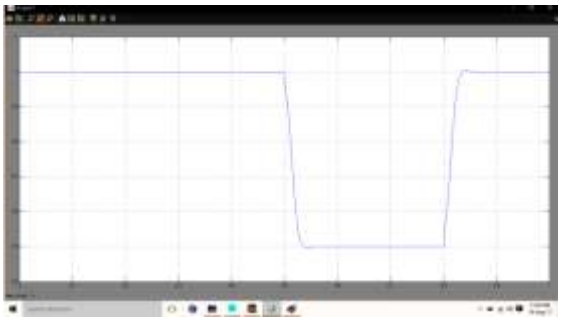

Fig:6(h) HVDC current

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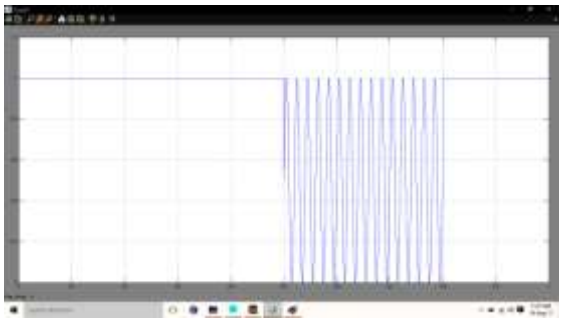

Fig:6(i) grid power

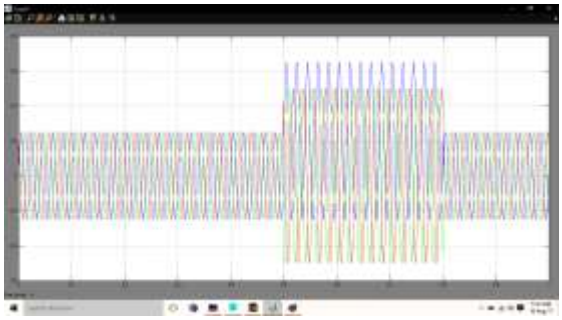

Fig:6(j) MMC upper arm power

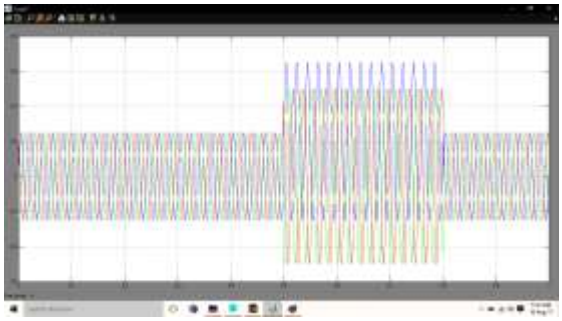

Fig:6(k) MMC lower arm power

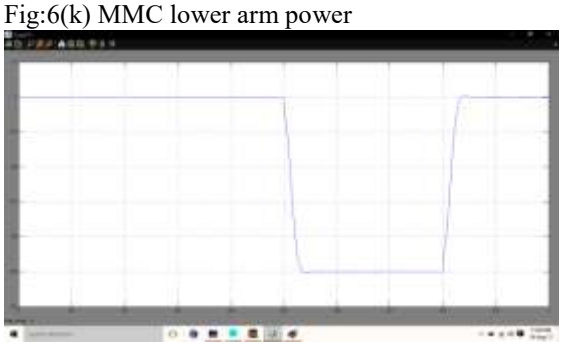

Fig:6(l) HVDC power

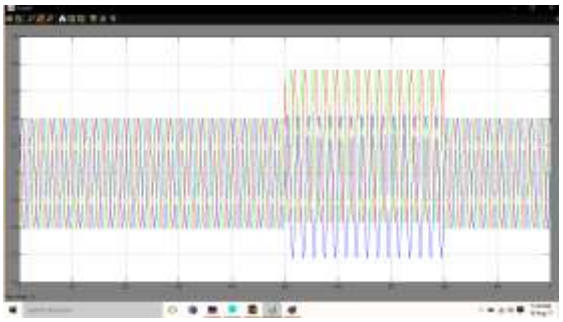

Fig:6(m) capacitor MMC upper arm

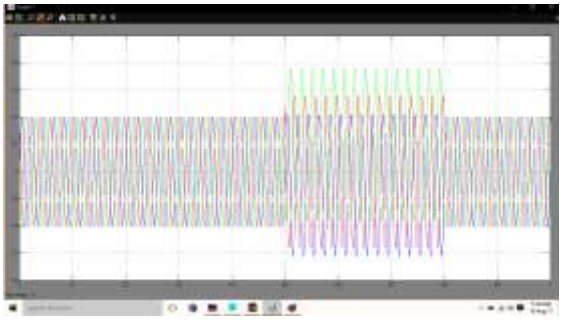

Fig:6(n) capacitor MMC lower arm

Fig. 6. Simulation results of the MMC operation. Voltage sag type C. Method 1 - Energy balancing disconnection.

CASE-C: Method 2 - Kernel-based approach.

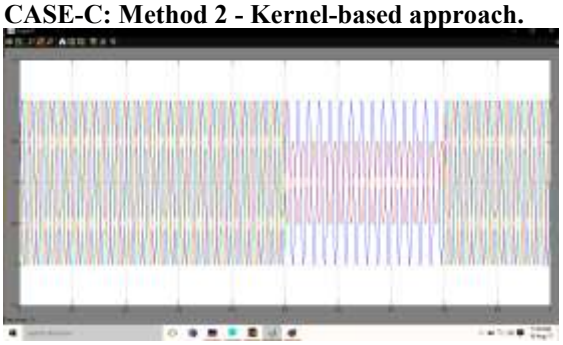

Fig:7(a) grid voltage

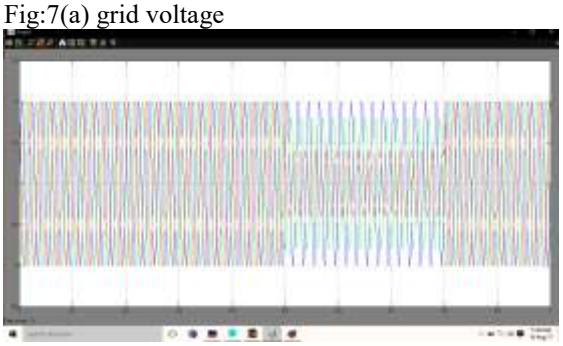

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Fig:7(b) MMC upper arm voltage

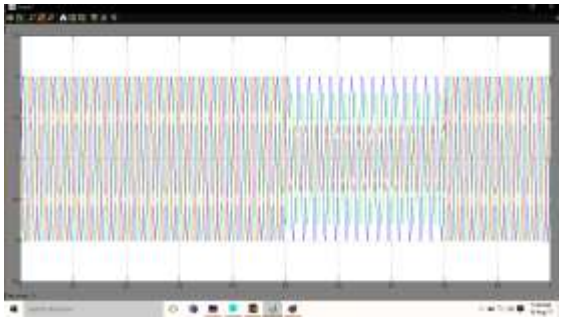

Fig:7(c) MMC lower arm voltage

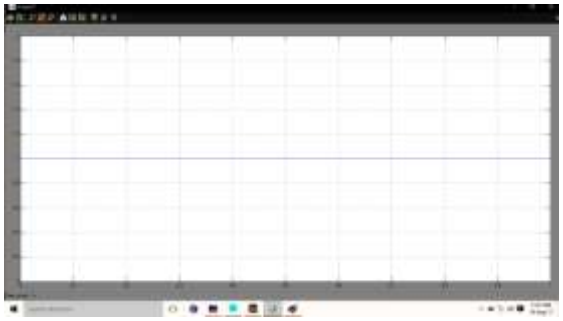

Fig:7(d) HVDC voltage

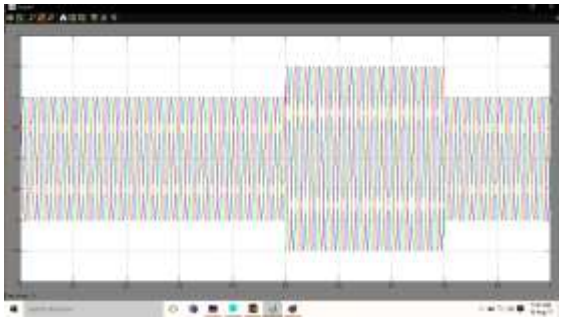

Fig:7(e) grid current

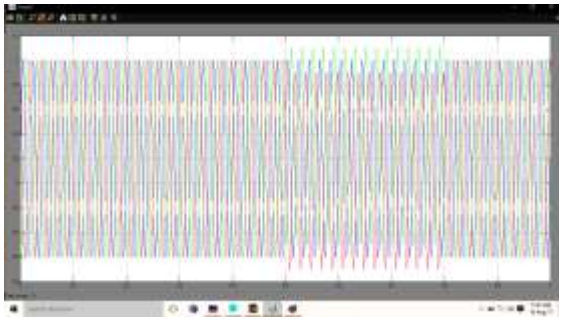

Fig:7(f) MMC upper arm current

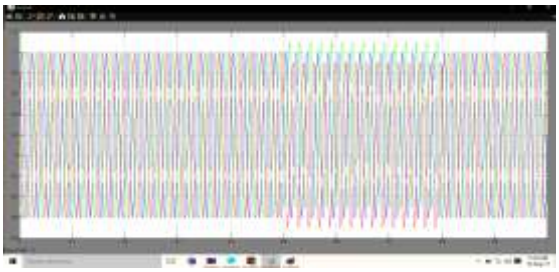

Fig:7(g) MMC lower arm current

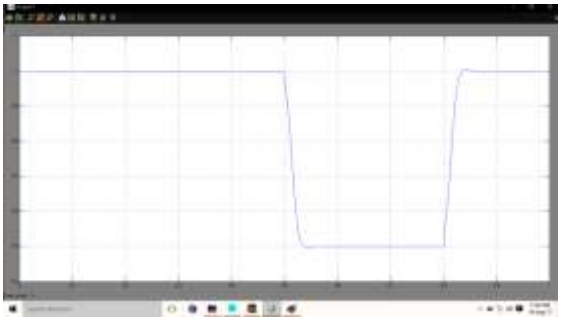

Fig:7(h) HVDC current

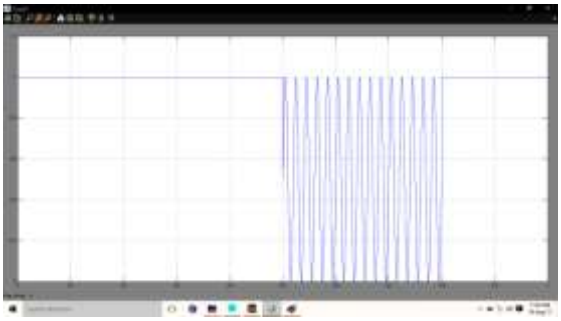

Fig:7(i) grid power

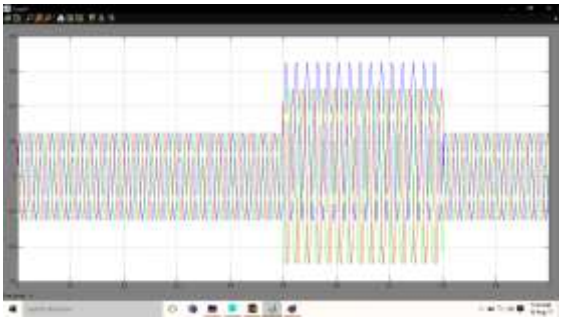

Fig:7(j) MMC upper arm power

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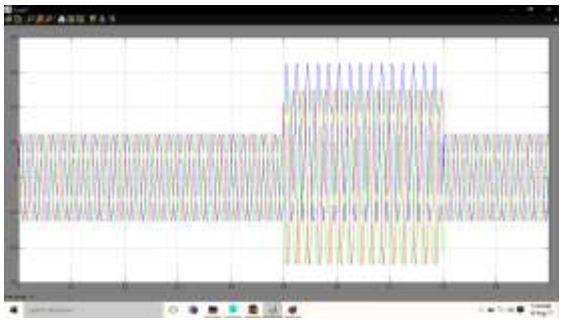

Fig:7(k) MMC lower arm power

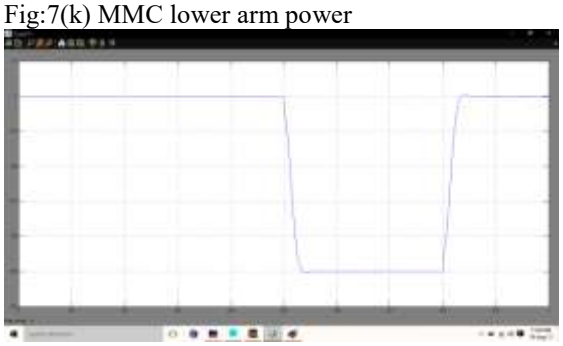

Fig:7(l) HVDC power

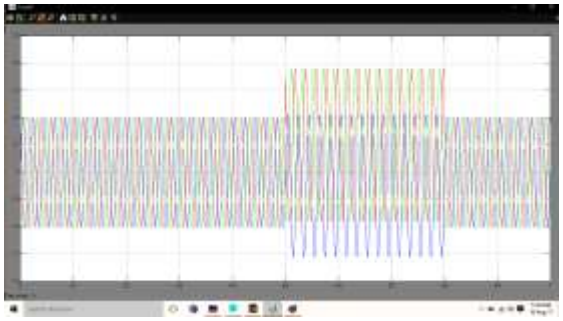

Fig:7(m) capacitor MMC upper arm

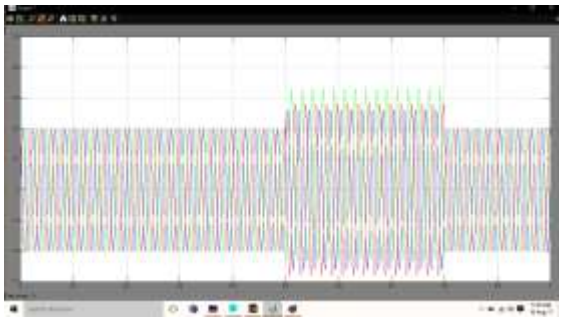

Fig:7(n) capacitor MMC lower arm

Fig. 7. Simulation results of the MMC operation. Voltage sag type C. Method 2 - Kernel-based approach.

CASE-D: Method 3 - Pseudoinverse-based approach.

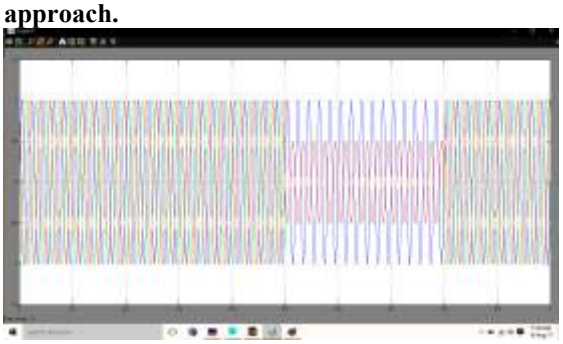

Fig:8(a) grid voltage

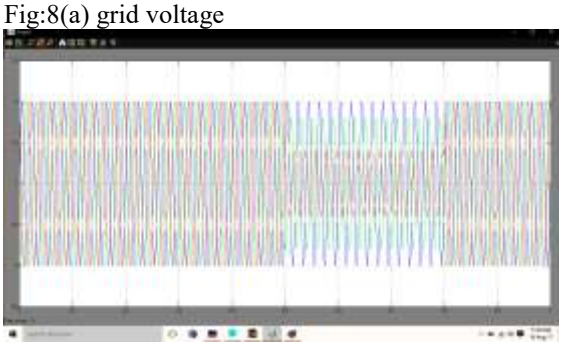

Fig:8(b) MMC upper arm voltage

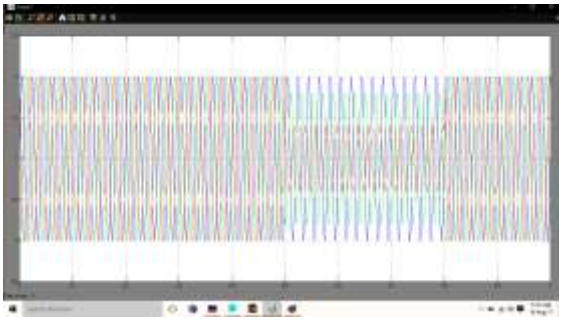

Fig:8(c) MMC lower arm voltage

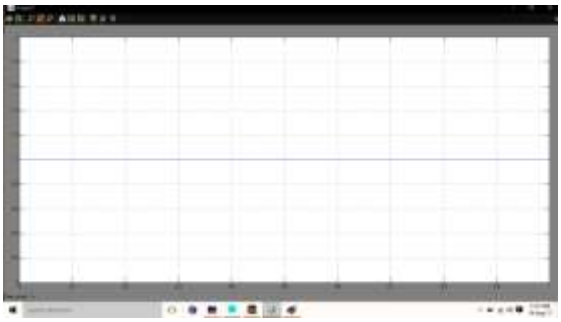

Fig:8(d) HVDC voltage

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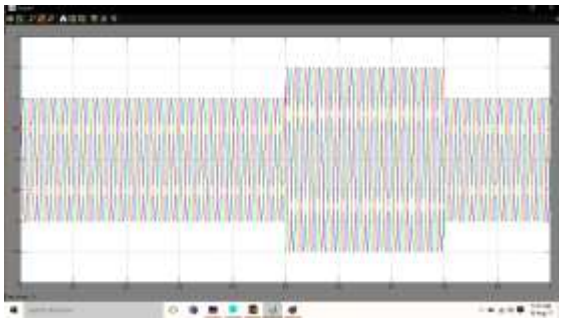

Fig:8(e) grid current

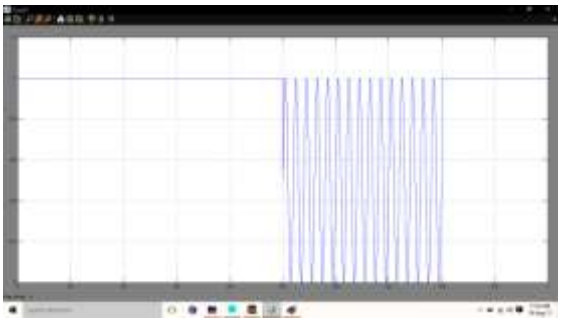

Fig:8(i) grid power

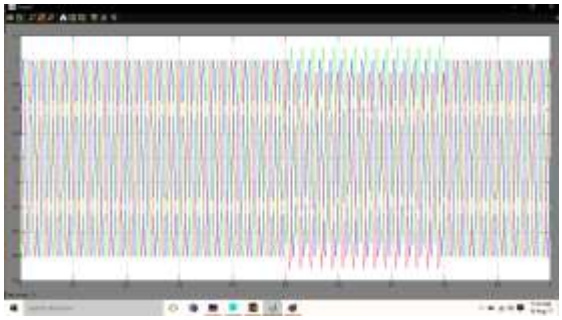

Fig:8(f) MMC upper arm current

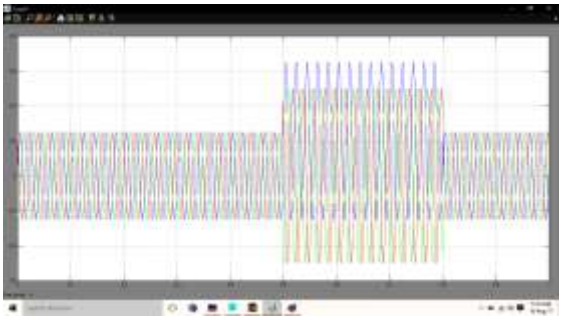

Fig:8(j) MMC upper arm power

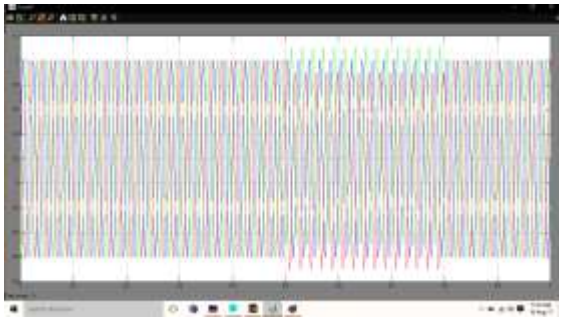

Fig:8(g) MMC lower arm current

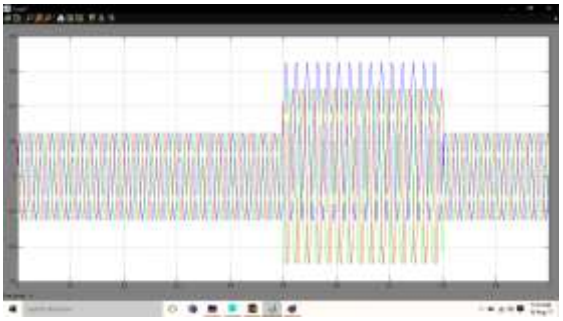

Fig:8(k) MMC lower arm power

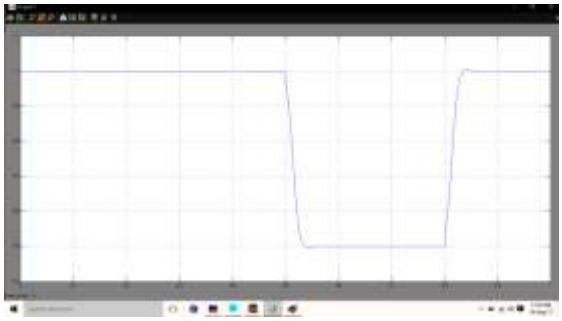

Fig:8(h) HVDC current

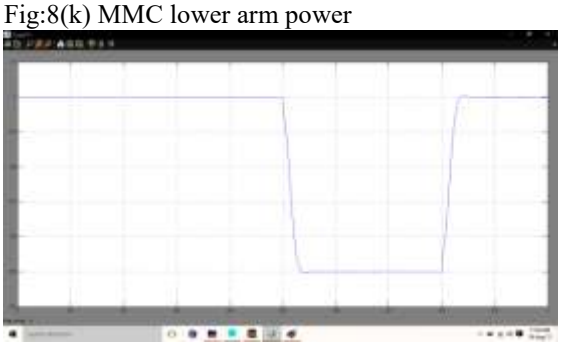

Fig:8(l) HVDC power

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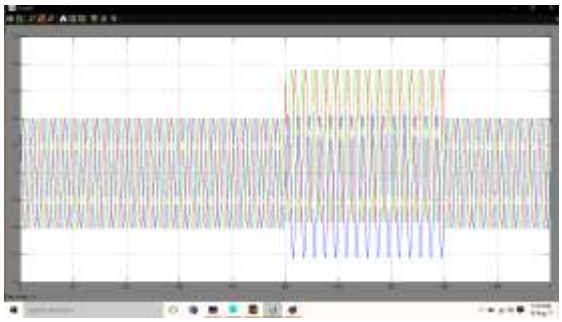

Fig:8(m) capacitor MMC upper arm

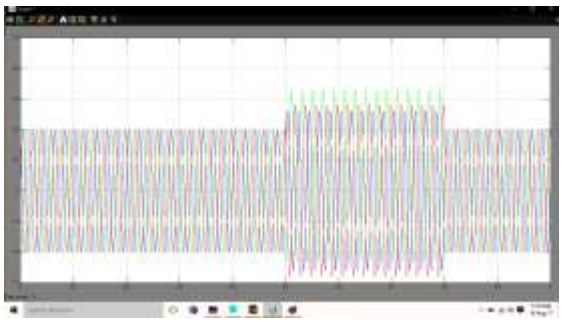

Fig:8(n) capacitor MMC lower arm

Fig. 8. Simulation results of the MMC operation. Voltage sag type C. Method 3 - Pseudoinverse-based approach.

CONCLUSION

Unbalanced voltage sags with singular voltage condition pose a challenge for the regulation of the energy balance between the upper and the lower arms of the converter. The analysis presented in this paper has shown how this specific condition may cause a singularity in the conventional current reference calculation. This singularity causes the current references to saturate, which compromises the performance of the energy balancing controllers. In order to overcome this issue, one option is to disable the energy balancing controller only during the fault, which makes the system stable but results in greater energy deviation. Alternatively, two new calculation methods have been presented which improve the deviation of the energy during the fault, regaining normal operation once the fault is cleared. The bases of the aforementioned methods have been discussed in detail and their benefits have been validated in a simulation model under all possible AC fault scenarios that produce the singular voltage condition.

REFERENCES

[1] O. Gomis-Bellmunt, J. Liang, J. Ekanayake, R. King, and N. Jenkins, "Topologies of multiterminal HVDC-VSC transmission for large offshore wind farms," *Elect. Power Syst. Res.*, vol. 81, no. 2, pp. 271–281, 2011.

[2] P. Wang, X.-P. Zhang, P. Coventry, and R. Zhang, "Start-up control of an offshore integrated MMC multi-terminal HVDC system with reduced dc voltage," *IEEE Trans. Power Syst.*, vol. 31, no. 4, pp. 2740–2751, Jul. 2016.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. Bologna Power Tech Conf.*, Bologna, Italy, Jun. 2003, vol. 3, 6 pp.

[4] J. Dorn, H. Huang, and D. Retzmann, "A new multilevel voltage-sourced converter topology for HVDC applications," in *Proc. CIGRE Session*, Paris, France, 2008, pp. 1–8.

[5] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSCHVDC transmission with cascaded two-level converters," in *Proc. Cigr´e Session*, Paris, France, 2010, Paper B4-B110.

[6] M. Merlin, T. Green, P. Mitcheson, D. Trainer, D. Critchley, and R. Crookes, "A new hybrid multi-level voltage-source converter with dc fault blocking capability," in *Proc. 9th IET Int. Conf. AC DC Power Transm.*, Oct. 2010, pp. 1–5.

[7] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Sep. 2009, pp. 1–10.

[8] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[9] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.